

REMARKS

This responds to the Office Action mailed on February 6, 2007.

Claim 1, 2, 4, 6, 8-12, 14, 16 and 18-22 are amended, no claims are canceled, and no claims are added; as a result, claims 1-22 are now pending in this application.

Nothing contained in the following summary is intended to change the specific language of the claims described, nor is the language of this summary to be construed so as to limit the scope of the claims in any way. Each claim amendment is supported by the specification and/or drawings.

Claims 1, 4, 6, 9 and 11 have been amended to more clearly define Applicant's claimed invention. Applicant's claimed invention is about a new method of advanced remote translation for use in a system having multi-nodes sharing an application. Specifically, Applicant's remote translation pertains to using an application virtual address space in a Remote Translation Table (RTT) on a local node to translate a virtual memory reference to a physical memory address for a remote node sharing the application with the local node. In contrast, the remote translation methods under Applicant's other applications, US Patent No. 6,922,766 (hereinafter "Scott") and US Patent Application No. 10/643,588 (hereinafter "Sheets"), transfer the virtual memory reference to a remote node's local memory to the remote node which then uses its local RTT to translate the memory reference.

Applicant accomplishes this distinction by constructing and using the application virtual address space in the RTT on each of the sharing nodes. When remote translation is enabled, each node exports its local virtual address space in its local RTT into the other sharing nodes' RTT. By doing this, each sharing node's RTT has the same application virtual address space covering all the sharing nodes' local memory translations. See e.g., Fig. 9. Therefore, once the application virtual address space is constructed and the remote translation mode is enabled, a local node does not have to transfer the virtual memory reference to the remote sharing node. Instead, the local node translates the virtual memory reference using the application virtual address loaded in its local RTT.

Amended claims 1, 4, 6, 9 and 11 are supported from the Specification as follows:

As described at Fig. 10 and p. 18, lines 3-23, Applicant teaches “a method of accessing shared memory in a computer system having a plurality of nodes, wherein each node includes a processor, a Translation Look-aside Buffer (TLB) associated with the processor and local memory wherein the local memory of each node includes a Remote Translation Table (RTT).”

As described at Figs. 8 & 9 and p. 18, lines 6-7, Applicant teaches distributing an application across the plurality of nodes.

As described at Figs. 8 & 9, p. 15, line 18 through p. 18, lines 2 and p. 18, lines 8-9, Applicant teaches building an application virtual address space in each of the plurality of nodes.

As described at Fig. 8, p. 16, lines 18-28 and p. 18, lines 9-12, Applicant teaches building a local virtual address space for the application in each of the plurality of nodes, wherein the local virtual address space translates a virtual address generated by the application executing on that node to a physical address in local memory for that node.

As described at Figs. 2-5 & 7, p. 9, lines 10-15 and p. 10, lines 27-30, Applicant teaches “the virtual address generated by the application executing on the node includes a node number of the node.”

As described at p 15, lines 22-29 and p. 17, lines 3-5, Applicant teaches determining whether remote translation should be enabled.

As described at Fig. 9 & 10, p. 15, line 27 though p. 16, line 2, p. 16, line 29 through p. 17, line 15 and p. 18, lines 12-13, Applicant teaches “if remote translation should be enabled, exporting the local virtual address space for each local node to the RTTs in each of the plurality of nodes.”

As described at p. 15, lines 12-29 and p. 17, lines 3-15, Applicant teaches “requesting that the operating system on each of the plurality of nodes enable remote translation.”

As described at Fig. 9 and p. lines 3-18, Applicant teaches “shadowing the local virtual address spaces for the node across the plurality of nodes.”

As described at Fig. 9 & 10 (block 1012), p. 15, line 29 through p. 16, line 2, p. 16, lines 8-11, p. 17, lines 14-15, p. 18, lines 14-19 and p. 19, line 28 through p. 20, line 3, Applicant teaches “if remote translation is enabled, translating a virtual memory reference to a physical memory address using the application virtual address space in the local RTT in each of the

plurality of nodes, wherein translating the virtual memory reference includes translating in a source node the node number of the application virtual address into a node address associated with a remote node of the plurality of nodes and translating bits of the application virtual address into a physical page address for the remote node.”

As described at Fig. 4 (block 408), p. 3, lines 18-23 and p. 10, lines 22-26, Applicant teaches, “if remote translation is not enabled, sending the virtual memory reference to the remote node and translating the virtual memory reference into a physical address in local memory for the remote node using the local virtual address space in the RTT on the remote node.”

As described at Fig. 4 (block 406), p. 18, lines 19-20 and p. 20, lines 6-8, Applicant further teaches and claims in claims 2, 4, 8 and 9, “the local virtual address space is read from the Translation Look-aside Buffer (TLB) on the node.”

As described at p. 15, line 29 through p. 16, line 5, p. 18, lines 20-23 and p. 19, lines 9-13, Applicant further teaches and claims in claims 3, 5, 7 and 10, “building an application virtual address space further includes performing a synchronization operation that causes at least some of the plurality of nodes to wait for all nodes to complete exporting their respective local virtual address spaces.”

As described at p. 16, lines 11-17 and p. 17, line 23 through p. 18, line 2, Applicant further teaches and claims in claims 18-22, “requesting the operating system enable remote translation handles requests to changes the application virtual address space configuration on a node-local basis, wherein handling requests includes disallowing an attempt to modify the application virtual address space outside scope of the local node.”

This summary does not provide an exhaustive or exclusive view of the present subject matter, and Applicant refers to the appended claims and their legal equivalents for a complete statement of the inventive subject matter.

§112 Rejection of the Claims

According to M.P.E.P. § 2163, citing *In re Oda*, 443 F.2d 1200, 170 USPQ 268 (CCPA 1971), newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure. An amendment to correct an obvious error does not constitute new matter where one skilled in the art would not only recognize the existence of the error in the specification, but also recognize the appropriate correction. *M.P.E.P.* § 2163, I. B.

The fundamental factual inquiry is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed. *Id.* See, e.g., *Vas-Cath, Inc.*, 935 F.2d at 1563-64, 19 USPQ2d at 1117.

When an explicit limitation in a claim "is not present in the written description whose benefit is sought it must be shown that a person of ordinary skill would have understood, at the time the patent application was filed, that the description requires that limitation." *Hyatt v. Boone*, 146 F.3d 1348, 1353, 47 USPQ2d 1128, 1131 (Fed. Cir. 1998). See also *In re Robins*, 429 F.2d 452, 456-57, 166 USPQ 552, 555 (CCPA 1970) ("Where no explicit description of a generic invention is to be found in the specification, ... mention of representative compounds may provide an implicit description upon which to base generic claim language."). *M.P.E.P.* § 2163, II, A. 3(b).

Claims 1-22 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Specifically, the Office Action states that the limitation in claims 1, 4, 6, 9 and 11, "translating the virtual memory reference into a physical address in the application virtual address space using the RTT on the local node, if the node number is not the local number and the remote translation is enabled..." is not supported by Applicant's Specification.

Claims 1, 4, 6, 9 and 11 have been amended to more clearly define Applicant's claimed invention. Applicant respectfully submits that, as noted in the discussion of the Summary of the claimed invention, Applicant teaches that local memory space in each node's RTT is exported to the RTT of other remote nodes associated with the local node through a distributed application when remote translation is enabled. See also Fig. 9 and p. 15, line 12 through p. 17, line 22. Applicant also teaches that, once an application virtual address is constructed by the exporting

process, translations for all local memory of the remote nodes sharing the application are shadowed in the RTT of each of the sharing nodes. See at Fig. 9 and p. 17, lines 3-15.

The disclosure conveys with reasonable clarity to one of ordinary skill in the art that, as of the filing date sought, Applicant was in possession of the limitation of “if remote translation is enabled, translating a virtual memory reference to a physical memory address using the application virtual address space in the local RTT in each of the plurality of nodes” as claimed, for example, in amended claim 1. In addition, as noted in the discussion of Summary of Claimed Invention, it is evident to a person of ordinary skill that the local node does not have to transfer the virtual memory reference to the remote node because the local node’s RTT has all translation information for local memory of the entire sharing nodes when each of the sharing nodes exports its local virtual address space to the sharing nodes’ RTT.

Therefore, the claim limitation in amended claim 1 is supported in the Specification through express or implicit disclosure as required by the MPEP and *In re Robins*. Similar arguments are applicable to the limitation in amended claims 4, 6, 9 and 11. Reconsideration is respectfully requested.

§103 Rejection of the Claims

Claims 1-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Schimmel (US 6,105,113), and in view of Scott et al. (US 6,925,547).

Applicant respectfully submits that neither Schimmel nor Scott, alone or in combination, teach or suggest a method and system for remote virtual address translation as taught by Applicant and claimed in claims 1-22. Claims 1, 4, 6, 9 and 11 have been amended to more clearly define Applicant’s claimed invention.

Schimmel describes a system and method for maintaining Translation Took-aside Buffer (TLB) consistency. Specifically, Schimmel describes automatically a method and system for keeping a TLB in a local node consistent with current changes in page table entries by its operating system without interrupting its CPU or operating system.

Scott describes a method for performing remote address translation in a multiprocessor system (Abstract, lines 1-2). Specifically, Scott describes an address translation method where a

virtual address for a remote node is sent to the remote node and translated into a physical address at the remote node using a translation look-aside buffer (TLB) (*id.* lines 2-19).

Neither Schimmel nor Scott, however, alone or in combination, teach or suggest following elements as taught by Applicant and claimed in amended claims 1, 4, 6, 9 and 11: (1) exporting the local virtual address space for each local node to the RTTs in each of the plurality of nodes sharing an application with the local node to build an application virtual address space; and (2) if remote translation is enabled, translating a virtual memory reference to a physical memory address using the application virtual address space in the local RTT in each of the plurality of nodes.

The Office Action states, first of all, that Schimmel teaches or suggests the exporting process as described and claimed by Applicant (Office Action, p. 6, lines 17-18). As support of this, the Office Action points to col. 1, lines 24-31 of Schimmel, which states:

In a virtual memory scheme, each process that is allocated a block of physical memory is also provided with a set of translations for translating virtual addresses to assigned physical addresses of the allocated block. Each set of translations can be stored in, for example, a page table. A page table can be associated with a specific user or shared by multiple users. Alternatively, reverse page table techniques can be employed.

Applicant respectfully disagrees. Although the cited portion explains general use of a page table for memory translation, it does not teach or suggest that the page table in a main memory contains virtual to physical address translation of local memory for remote nodes other than its own local node. In contrast, as noted in the discussion of §112 rejection, Applicant explicitly teaches, and claims in amended claims 1, 4, 6, 9 and 11 that each node exports its local address space to each of a plurality of remote nodes associated with the local node through distribution of an application. Applicant is unable to find such a teaching in any of the cited references.

In addition, the Office Action states that Schimmel teaches or suggests translating a virtual memory reference to a physical address in a remote node using the RTT in a local node (Office Action, p. 8, lines 3-8). As support of this, the Office Action points to col. 4, lines 8-13, col. 7, lines 50-67 and col. 8, lines 1-67 of Schimmel, part of which states:

(col. 4, lines 8-13) In operation, when a CPU requires a physical memory address that is associated with a virtual memory address, the CPU first searches the virtual address tag of the TLB table. If a valid translation is not found in the TLB table, the translation is

retrieved from a cache or from main memory and a copy of the translation is placed in the TLB table.

(col. 7, line 49 through col. 8, line 67) Referring to FIG. 5, a virtual memory address-to-physical main memory address translation scheme 510 is illustrated...Each user or application that is allocated a portion of physical memory can be provided with a separate page table 610. In some cases, page tables can be shared....Thus, a reference F4 will result in a page table miss or page fault and F4 will have to be retrieved from 514....

Applicant respectfully disagrees. First of all, as discussed above, none of the cited portions teach or suggest that the page tables of Schimmel contain virtual to physical address translation for other remote nodes. Therefore, the page tables on the local main memory are not used to translate a virtual memory reference for a remote node into a physical address in the remote node. In contrast, as noted in the discussion of § 112 rejections, Applicant claims in amended claims 1, 4, 6, 9 and 11 that the application virtual address space in the local RTT in each of the plurality of nodes is used to translate a virtual address reference from the local node to a remote sharing node if remote translation mode is enabled. Applicant is unable to find such a teaching in any of the cited references.

Furthermore, Applicant also teaches, for example, at p. 6, lines 19-21 and p. 15, lines, 12-29, and claims in claims 1, 4, 6, 9 and 11 that Applicant's invention translates a virtual address reference for a remote node differently depending on remote translation mode. Under Applicant's claimed invention, if remote translation is not enabled, the virtual memory address for the remote node is sent to the remote node and translated to a physical address in the remote node using the local virtual address space in the RTT on the remote node instead of using the application virtual address space in the RTT on the requesting local node. *Id.* Applicant is unable to find such teachings or suggestions in any of the cited references.

For the reasons discusses above, neither Schimmel nor Scott, alone or in combination, teach or suggest a method and system for translating remote address references as taught by Applicant and claimed in amended claims 1, 4, 6, 9 and 11. Reconsideration is respectfully requested.

With regard to claims 3, 5, 7 and 10. Claims 3, 5, 7 and 10 are patentable as being dependent on a patentable base claim. In addition, neither Schimmel nor Scott, alone or in combination, teach or suggest synchronizing nodes for completion of exporting RTTs among associated nodes as taught by Applicant and claimed in claims 3, 5, 7 and 10.

The Office Action states that “in order for the remote translation mechanism disclosed by Schimmel to work and function properly, it is inherent that the RTT at all the nodes be initialized and synchronized first before any reference to a memory location resides at a remote node can be served” (p. 10, lines 5).

Applicant respectfully disagrees. First of all, as discussed above, it is not clear from a reading of Schimmel whether the page tables in each node under Schimmel’s approach contain virtual to physical address translation for other remote nodes. Schimmel does not teach or suggest exporting all local translations in each node to each of the associated nodes to build an application virtual address space containing all translation information for all of the associated nodes. Therefore, it would not necessarily be obvious to one of ordinary skill in the art at the time of invention to selectively synchronize RTTs of nodes that share an application as taught by Applicant and claimed in claims 3, 5, 7 and 10. Reconsideration is respectfully requested.

With regard to claims 18-22, claims 18-22 are patentable as being dependent on a patentable base claim. In addition, neither Schimmel nor Scott, alone or in combination, teach or suggest handling requests to change the application virtual address space configuration on a node-local basis as taught by Applicant and claimed in claims 18-22. Reconsideration is respectfully requested.

With regard to claims 2, 8 and 12-17, claims 12-17 are patentable as being dependent on a patentable base claim.

Double Patenting Rejection

According to M.P.E.P. § 804, which cites *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993), a rejection based on nonstatutory double patenting is based on a judicially created doctrine grounded in public policy so as to prevent the unjustified or improper timewise extension of the right to exclude granted by a patent. In determining whether a nonstatutory basis exists for a double patenting rejection, the factual inquires set forth for determining obviousness under 35 U.S.C. 103 in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966) must be shown: (A) the scope and content of a patent claim relative to a claim in the application at issue; (B) the differences between the scope and content of the patent claim as determined in (A) and the claim in the application at issue; (C) the level of ordinary skill in the pertinent art; and (D) evaluation of any objective indicia of nonobviousness. In addition, any obviousness-type double patenting rejection should make clear: (A) the differences between the inventions defined by the conflicting claims – a claim in the patent compared to a claim in the application; and (B) the reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim at issue would have been an obvious variation of the invention defined in a claim in the patent.

If the application at issue is the later filed application or both are filed on the same day, only a one-way determination of obviousness is needed in resolving the issue of double patenting, i.e., whether the invention defined in a claim in the application would have been an obvious variation of the invention defined in a claim in the patent. See, e.g., *In re Berg*, 140 F.3d 1438, 46 USPQ2d 1226 (Fed. Cir. 1998). Similarly, even if the application at issue is the earlier filed application, only a one-way determination of obviousness is needed to support a double patenting rejection in the absence of a finding: (A) of administrative delay on the part of the Office causing delay in prosecution of the earlier filed application; and (B) that applicant could not have filed the conflicting claims in a single (i.e., the earlier filed) application. See M.P.E.P § 804, ¶ II.B.1.(b).

Claims 1-2, 4, 6, 8-9 and 11 were rejected under judicially created doctrine of anticipation-type double patenting as being anticipated by claims 1-35 of U.S. Patent No. 6,922,766 (hereinafter ‘766).

As noted above, determination of one-way obviousness applies here. When applying one-way obviousness test, the Examiner must establish a *prima facie* case of obviousness under 35 U.S.C. § 103 as in the obviousness discussion above.

Applicant respectfully submits that the present claims are patentably distinct from the claims of ‘766. Each of the independent claims in ‘766 includes transmitting virtual memory reference from a local node for local memory for a remote node to the remote node which then translates the virtual addresses to a physical address in the remote node using the RTT on the remote node. Unlike the claims in ‘766, for example, Applicant’s claimed invention translates a memory reference to a physical address for a remote node differently depending on whether remote translation is enabled. Under Applicant’s amended claims, a local node translates a virtual memory address for a remote node on the local node using an application virtual address space in the local RTT on the local node if remote translation is enabled. To accomplish this, Applicant claims that local memory space for each of the plurality of nodes is exported to the RTTs of all remote nodes sharing an application with the local node. Claims in ‘766 do not contain such limitations in its claims.

The Office Action, therefore, has failed to establish a *prima facie* case of obviousness and thereby failed to show satisfying one-way obviousness test as required by *Graham* and *M.P.E.P.* as noted above. In conclusion, Applicant’s claimed invention is not anticipated by and patentably distinct from claims of ‘766. Reconsideration is respectfully requested.

Claims 1-2, 4, 6, 8-9, and 11 were rejected under the judicially created doctrine of “anticipation-type double patenting” as being unpatentable over claims 1, 2, 4, 6, 8-9, and 11 of U.S. App. Serial No. 10/643,588 (hereinafter ‘588).

As noted above, determination of one-way obviousness applies here. When applying one-way obviousness test, the Examiner must establish a *prima facie* case of obviousness under 35 U.S.C. § 103 as in the obviousness discussion above.

Applicant respectfully submits that the present claims are patentably distinct from the claims of '588. Each of the independent claims in '588 includes transmitting a remote node virtual memory address from a local node to the remote node which then translates the remote virtual address to a physical address in the remote node using ERTT Segment on the remote node. Unlike the claims in '588, for example, Applicant's claimed invention translates a memory reference to a physical address for a remote node differently depending on whether remote translation is enabled. Under Applicant's amended claims, a local node translates a virtual memory address for a remote node on the local node using the application virtual address space in the local RTT on the local node if remote translation is enabled. To accomplish this, Applicant claims that local memory space for each node is exported to each remote node associated with the local node through an application. Claims in '588 do not contain such limitations in its claims.

The Office Action, therefore, has failed to establish a *prima facie* case of obviousness and thereby failed to show satisfying one-way obviousness test as required by *Graham* and *M.P.E.P.* as noted above. In conclusion, Applicant's claimed invention is not anticipated by and patentably distinct from claims of '588. Reconsideration is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.116 – EXPEDITED PROCEDURE

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priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 17 day of April 2007.

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